

Analysis of Current Control Techniques on Bridgeless Interleaved Boost DC-DC Converter to Improve Power Quality

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Abstract—This paper presents the comparison of various current control techniques employed for a bridgeless interleaved boost converter for improving the power quality. The major control strategies discussed in this paper are: peak current, average current mode and borderline current control. These strategies are implemented in MATLAB/SIMULINK and the performance of the proposed converter is compared under open loop and closed loop operation. From the results, the input current waveform was close to sinusoidal implying high power factor and reduced harmonics for borderline control.

Keywords- Bridgeless IBC, THD, Power Factor & , Current Control Techniques

I. INTRODUCTION

For automotive and battery charging applications, a regulated DC supply is required and since AC supplies are more commonly available, a suitable AC-DC converter becomes mandatory for such applications. These AC-DC converters involve a number of non-linear devices which reduce the system power factor and introduce harmonics in the power system leading to adverse effects. Hence it is essential to use a suitable power factor correction technique to condition the supply current. This paper presents the design and implementation of one such Active Power Factor corrected AC-DC Converter topology, which results in an improved supply power factor and reduced line current harmonics. A novel converter topology, namely the Bridgeless Interleaved Boost Topology for active power factor correction, along with a closed loop current control technique to condition the supply current has been proposed in this paper. Various current control techniques have been investigated for the proposed topology and the supply side parameters are computed to show the effectiveness of the current shaping methods. Simulation studies are carried out in MATLAB/SIMULINK and the results are presented.

II. BRIDGELESS INTERLEAVED BOOST CONVERTER

The Bridgeless Interleaved Boost Converter (IBC) topology for active power factor correction consists of a number of boost converters operating in parallel. The input diode bridge rectifier stage is eliminated while still maintaining the classic IBC structure. This topology affords a number of advantages in comparison to the conventional topologies [1-3]. It addresses the heat management problem caused by the input diode rectifier stage of IBC. In effect, the bridgeless

IBC topology combines the benefits of both the bridgeless topology and the interleaved structure. In the Bridgeless Interleaved Boost Converter topology, the rectifier stage is integrated with the high frequency converter. Due to the elimination of the bridge rectifier stage, the circuit becomes less bulky. Interleaving leads to an increase in the frequency of input current ripples and hence a reduction in the weight and volume of EMI filters required. The conduction losses are greatly reduced due to the presence of fewer number of semiconductor devices in each conduction path. In comparison to a two-phase IBC, a two-phase bridgeless IBC topology uses two extra MOSFETs and fast diodes, instead of the four slow diodes in the bridge rectifier stage. This converter topology thus affords the maximum efficiency due to the combined merits of interleaving and the bridgeless structure.

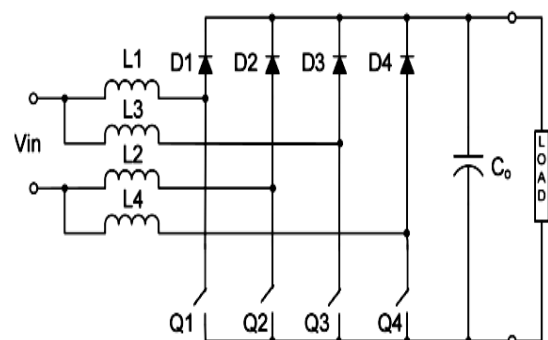


Fig.1 Bridgeless Interleaved Boost DC-DC Converter

A. Circuit operation

For analysis of the topology, the circuit is separated into two half cycles. Q_1 and Q_2 are turned on at the same instant and Q_3 and Q_4 are turned on at the same instant which is 180° out of phase with respect to the instants of Q_1 and Q_2 . During the positive half cycle, Q_1 and Q_2 are turned ON and

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the current flows through L_1 , Q_1 , Q_2 and L_2 thereby storing energy in L_1 and L_2 . When Q_1 and Q_2 are turned off, the energy stored in L_1 and L_2 are released as current through D_1 , load, body diode of Q_2 and is fed back to the mains. Similarly, with a shift of 180° , Q_3 and Q_4 are turned ON and energy is stored in L_3 and L_4 via Q_3 and Q_4 . During the negative half cycle, Q_4 and Q_2 are turned ON, energy gets stored in L_2 and L_1 for the first phase and L_4 and L_3 for the next phase and gets released as current which flows through D_2 (D_4), load, body diode of Q_1 (Q_3) and back to mains. A new loss has been introduced in the intrinsic body diodes of the FETs, but since input bridge rectifiers are eliminated, there is some efficiency gain in overall performance of the topology [4-6].

Overall, the MOSFETs are under more stress in bridgeless IBC topology, but the total loss for the proposed bridgeless interleaved boost are 40% lower than the conventional boost, 27% lower than the bridgeless boost and 32% lower than the interleaved boost. Since the bridge rectifier losses are so large, it is expected that bridgeless interleaved boost converter would have the least power losses in comparison to the conventional topologies, discussed in the literature. It is to be noted that the losses in the input bridge rectifiers constitute 63% of total losses in conventional PFC converter and 71% of total losses in interleaved PFC converter. Therefore eliminating the input bridges in PFC converters is justified despite the fact that new losses are introduced. The bridgeless IBC topology is chosen for final implementation purposes due to its various merits, as discussed above.

III. CURRENT CONTROL TECHNIQUES FOR SHAPING THE SUPPLY CURRENT

The power factor obtained with the AC-DC converter topologies can further be improved using wave shaping techniques to condition the supply current. The power factor is found to be the highest in case of the bridgeless IBC topology in the open loop configuration. To further improve power factor and make it closer to unity, feed forward and feedback loops are introduced in the circuit to detect and shape the supply current and to reduce its harmonic distortion. The current control strategies are classified into two modes, namely the Discontinuous Inductor Current Mode (DICM) where the inductor current reaches zero during a cycle and Continuous Inductor Current Mode (CICM) where the inductor current never reaches zero during a cycle and there is always energy stored in the inductor. Some of the Continuous Inductor Current Mode control strategies are: Peak Current Control, Average Current Control and Borderline Current Control [7-8].

A. Peak Current Control

In this mode of control (refer Fig.2), an R-S flip flop is used to toggle the power switches. The flip flop is set for every

falling edge of the clock input. The switches are switched ON at a constant frequency. The current through the inductor increases practically linearly. When it reaches a reference value I_{ref} , the switch is turned OFF. Peak detector circuits are used to detect the peak current and the flip flop is reset which turns the power switches OFF. Peak current control is inherently unstable when the duty ratio of the converter exceeds 50% due to the presence of sub-harmonic oscillations [9]. So, a compensating ramp is used along with the peak detector circuit when the duty ratio exceeds 50%. As seen in the figure I_{ref} is generated by multiplying the output voltage error amplifier and the input sinusoidal reference current. When the inductor current reaches I_{ref} , the flip flop is reset and power switch is turned off. The compensating ramp is avoided in this work since the duty ratio is equal to 50%.

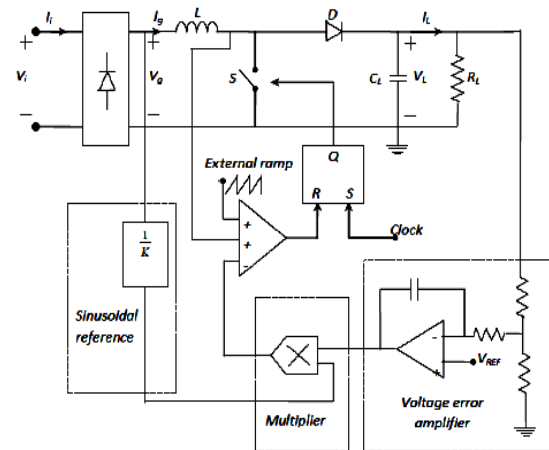


Fig. 2 Block Diagram of Peak Current Control Mode

The following are the advantages and disadvantages of peak current mode control:

Advantages

- The switches are triggered at a constant frequency.
- It is enough that only the switch current is sensed and it is accomplished by a current transformer thereby eliminating the losses due to sensing resistor.
- Switch current limiting is accomplished thereby protecting the power switches

Disadvantages

- Sub-harmonic oscillations are introduced in the cases where duty cycle is greater than 50%. An extra compensating ramp is required.
- Any noise spike in the input current can turn the switch OFF immediately. The control is highly sensitive to communication noises.

The MATLAB implementation of this control mode and the resulting supply voltage and current waveforms are shown in Figs. 3 & 4

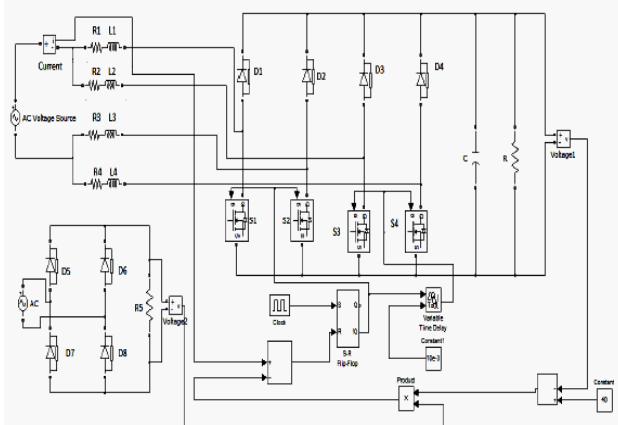


Fig.3 MATLAB circuit of Peak Current Control Mode with Bridgeless Interleaved Boost Converter Topology

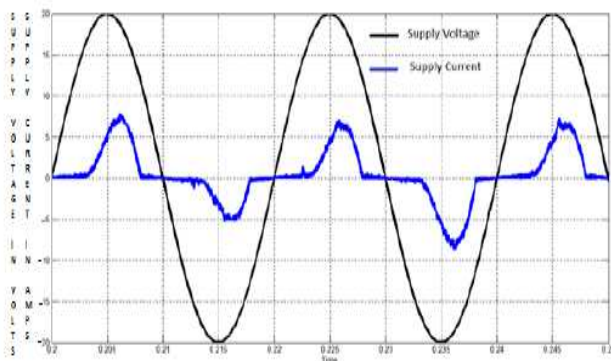


Fig.4 Supply Voltage and Supply Current Waveforms

B.Average Current Control

The technique of average current mode control overcomes the low current loop gain problem of the peak control mode by introducing a high gain integrating current error amplifier in the current loop as shown in Fig.5. Average current mode control differs from peak current mode control in that it attempts to control the average value of the current to follow a reference as opposed to controlling the switch peak current. The fundamental notion is to introduce a closed loop of average inductor current state variable as an inner loop in a dual loop control system. In this inner loop, the intent is to re-shape the inductor current of peak Current Mode, so as to improve it with higher gain at the low frequency region and extend its cross over frequency. In short, average current mode control is a two loop control method, inner loop being the current and the outer loop being the voltage loop for power electronic converters.

Here the inductor current is sensed and filtered by a current error amplifier whose output drives a PWM modulator. The control methods reviewed in the previous sections all suffer from high sensitivity to commutation noise. The technique of average current-mode control addresses this issue by introducing a current compensator in the current feedback

loop that allows a more sinusoidal input current in the converter. The inner current loop compensator in this control technique attempts to minimize the error between sensed input current and the current reference (the current reference is obtained in the same way as in peak current control). This ensures a unity power factor and the reduction of higher order supply current harmonics. Hence, average current mode control is generally considered as the best control approach for AC/DC PFC converters especially, single-stage PFC converters. Since the input current tracks an average reference signal, the PFC converter operates in CCM with this control technique. Like peak current control, the current reference in average current-mode control is the product of input voltage and the outer voltage loop compensator.

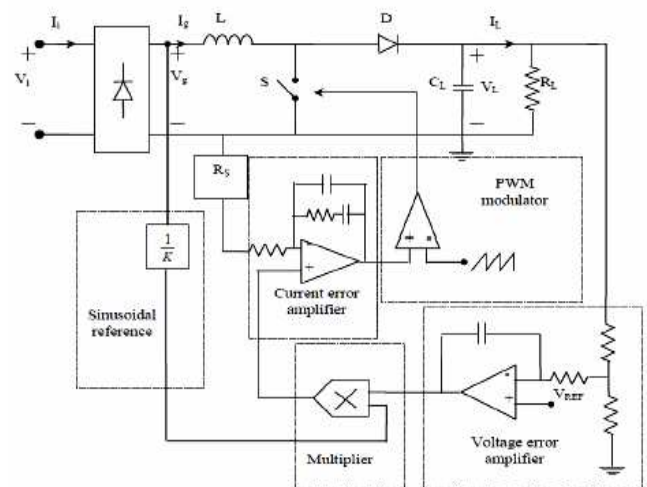


Fig. 5 Block Diagram of Average Current Control Mode

The following are the advantages and disadvantages of average current mode control:

Advantages

- Average current mode control has better noise immunity compared to peak current control.
- Fixed switching frequency operation and there is no need for slope compensation as the modulator ramp/carrier waveform provides the required compensation.
- Better accuracy.

Disadvantages

- The scheme does not provide immediate switch current limit as in the case of peak current control.
- Need for a current error amplifier compared to peak current control.
- Dynamic response is slow.

The MATLAB implementation of this control mode and the resulting supply voltage and current waveforms are shown in Figs.6 & 7.

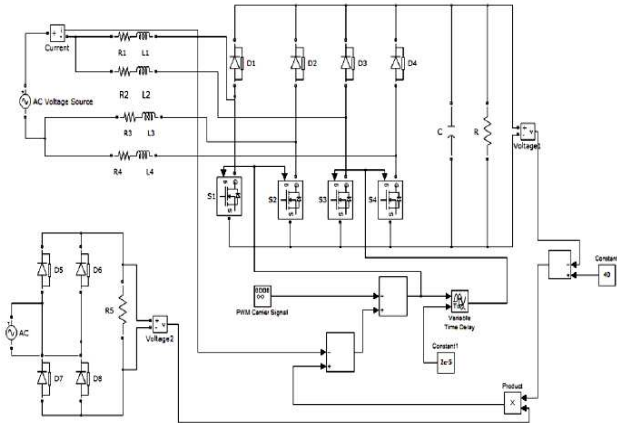


Fig.6 MATLAB Circuit of Average Current Control Mode with Bridgeless Interleaved Boost Converter Topology

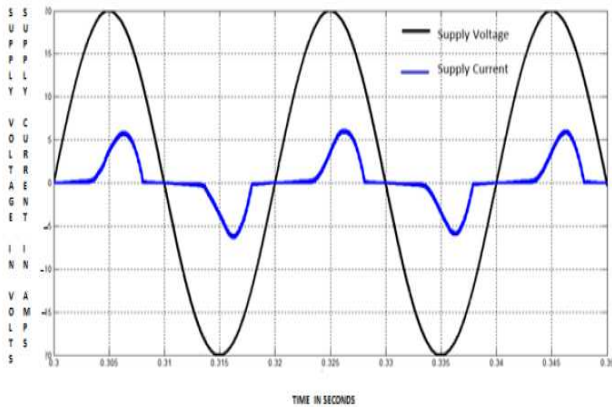


Fig.7 Supply Voltage and Supply Current Waveforms

B. Borderline Control

In this mode of control, the switch on-time is kept constant during the line cycle and the switch is turned on when the inductor current falls to zero, so that the converter operates at the boundary between Continuous and Discontinuous Inductor Current Mode (CICM,DICM)[10-11]. This allows the switch to be turned on when the input inductor current reaches zero and to be on until the input inductor reaches the upper reference value. The frequency of this type of controller varies with line and load. At high line and load, the frequency is at maximum but also varies throughout the line cycle (high frequency near zero crossing and low frequency near the peak). The principle scheme is shown in Fig. 8. The instantaneous input current is constituted by a sequence of triangles whose peaks are proportional to the line voltage. Thus, the average input current becomes proportional to the line voltage without duty-cycle modulation during the line cycle. Borderline conduction mode (or Critical conduction mode) operation is the most popular solution for low power applications. It is characterized by a variable frequency control scheme in which the inductor current ramps to twice the desired average value, ramps down to zero, then immediately ramps

positive again. This control technique is referred to as "automatic current shaper". The same control strategy can be generated, without using a multiplier, by modulating the switch on-time duration according to the output signal of the voltage error amplifier[12]. In this case switch current sensing can be eliminated.

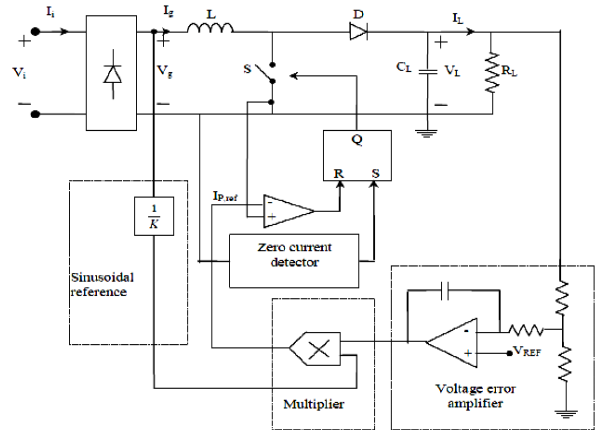


Fig.8 Borderline control with Boost topology

Advantages

- Simple Control Scheme. The application requires few external components
- Compensating ramp is not required
- Current Error Amplifier is not required

Disadvantages

- Large switching frequency variations
- Inductor voltage must be sensed in order to detect the zeroing of the inductor current
- For controllers in which the switch current is sensed, control is sensitive to commutation noises.

The MATLAB implementation of this control mode and the resulting supply voltage and current waveforms are shown in Figs.9 & 10.

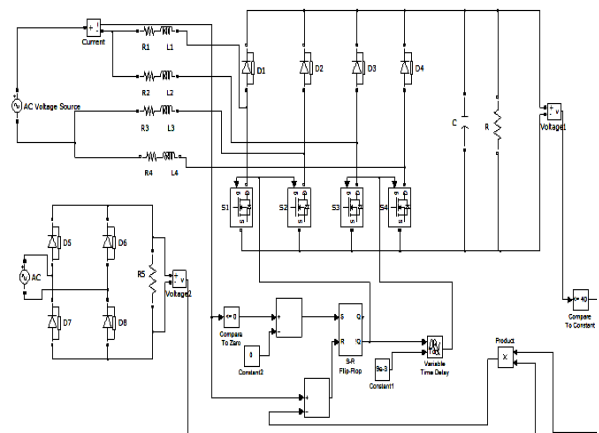


Fig.9 MATLAB Circuit of Borderline Control Mode with Bridgeless Interleaved Boost Converter Topology

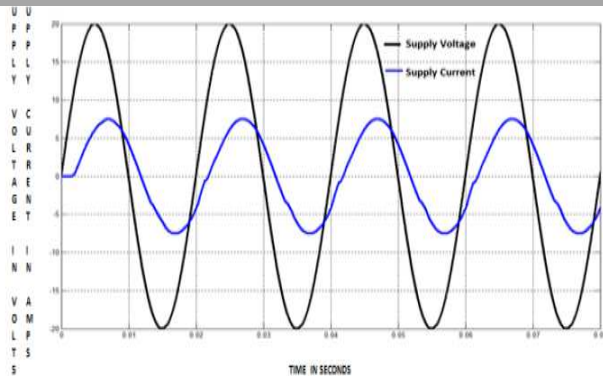


Fig.10 Supply Voltage and Supply Current Waveform
From Fig.10, it is found that the borderline control has improved the spectral quality of the supply current compared to the average current technique. The various performance parameters are calculated which is discussed in the next section.

VI. ANALYSIS OF PERFORMANCE PARAMETERS FOR BRIDGELESS IBC RECTIFIER

The performance parameters for the proposed topology are discussed as follows:

A. Total Harmonic Distortion (THD)

The total harmonic distortion or THD is a measurement of the harmonic distortion present in a signal and is defined as the ratio of the square root of the sum of the squares of all harmonic components to the fundamental frequency component. Mathematically, it is represented as:

$$THD_i = \frac{\sqrt{\sum_{n=2}^{\infty} I_{n,rms}^2}}{I_{1,rms}}$$

B. Distortion Factor or Purity Factor (Kp)

The distortion factor describes how the harmonic distortion of a load current decreases the average power transferred to the load. Mathematically, it is represented as:

$$K_p = \frac{1}{\sqrt{1 + THD^2}}$$

C. Displacement factor (Kd):

Displacement factor is defined as the cosine of the angle (ϕ) between the voltage and current.

$$K_d = \cos \phi$$

D. Power Factor (PF)

Power factor is defined as the product of the Distortion Factor and the Displacement Factor.

$$PF = K_p * K_d$$

The design parameters for the bridgeless IBC are $f_s = 25\text{kHz}$, $V_{in} = 20\text{V}$, $V_o = 40\text{V}$, duty ratio = 0.5, $L_1 = 667\mu\text{H}$, $C = 760\mu\text{F}$, $R = 47.06\text{ ohms}$. The following table

shows the consolidated comparative results of the performance parameters of the various current control strategies discussed in this paper.

Table : 1

Topology	THD (%)	Distortion Factor(kp)	Displacement Factor (kd)	Power Factor
Open loop	68.43	0.8252	0.9995	0.8248
Peak Current	55.16	0.8756	0.9995	0.8752
Average Current	50.75	0.8917	0.9998	0.8915
Borderline	13.02	0.9916	0.9916	0.8689

Comparative results of the performance parameters of the Bridgeless Interleaved Boost Converter Topology with the various current control strategies incorporated From the above table, it can be inferred that the border line control technique is the most preferable as it affords the low THD for the supply current and improved power factor.

V. CONCLUSION

A two-phase bridgeless interleaved boost converter has been investigated and it is found that the proposed topology has improved the spectral quality of the supply current and better

power factor. The current control techniques for improving the power quality for bridgeless interleaved boost converter have been analyzed. A comparative analysis of peak current, average current and borderline current control has been carried out by implementing these strategies in MATLAB-SIMULINK. The simulation results obtained show that the borderline current control offers the power factor very close to unity and the supply current THD is about 13.02% compared to the other techniques.

REFERENCES

- [1]. Balogh.L and Redl.R, Power-factor correction with interleaved boost converters in continuous-inductor-current mode, Applied Power Electronics Conference and Exposition (APEC), Eighth Annual Conference Proceedings, Print ISBN: 0-7803-0983-9, pp. 168 – 174, 1993.
- [2]. Chen Zhou and Milan M. Jovanovic , “Design Trade offs in Continuous Current-Mode Controlled Boost Power-Factor Correction Circuits - Seventh International High Frequency Power Conversion (HFPC) Conf., San Diego, CA, pp. 209-220, 2011.
- [3]. Hasaneen B.M. and Mohammed, A.A.E., Design and simulation of DC/DC boost converter, 12th International Middle-East Power System Conference, pp.335 – 340, 2008.
- [4]. Kurma Sai Mallika , Topological Issues In Single Phase Power Factor Correction – Department of Electrical Engineering National Institute of Technology, Rourkela-769008, 2007.

- [5]. Lai, J. S., , “Design consideration for Power Factor Correction Boost converter operating at the Boundary of Continuous Conduction mode and Discontinuous Conduction mode - Proc. of IEEE Applied Power Electronics Conference(APEC) ,pp. 267-273, 1993.
- [6]. Lee . P, Lee . Y, D.K.W. Cheng and X.Liu, ”Steady-state analysis of an interleaved boost converter with coupled inductors - IEEE Trans. Industrial Electronics”, 2000, pp. 787–79.
- [7]. Jian Li , Current-Mode Control: Modelling and its Digital Application- Dissertation, Virginia Polytechnic Institute and State University, Blacksburg, Virginia, 2009.
- [8]. Kamran Rezaei, “A Control Scheme for an AC-DC Single-Stage Buck-Boost PFC Converter with Improved Output Ripple Reduction”, Dissertation, The School of Graduate and Postdoctoral Studies, University of Western Ontario - Electronic Thesis and Dissertation, 2012.
- [9]. J. P Gegner, C. Q. Lee, Linear Peak Current Mode Control: A Simple Active Power Factor Correction Control Technique for Continuous Conduction Mode, PESC Conf.Proc., 1996, pp. 196-202.
- [10]. J. R. Rajagopalan, P. Nara, F. C. Lee, A generalized Technique for Derivation of Average Current Mode Control Laws for Power Factor Correction without Input Voltage sensing, APEC Conf. Proc., 1997, pp. 81-87.
- [11]. Rossetto. L., Spiazzi G., Tenti P., “Control techniques for power factor correction converters”, Power Electronics and Motion Control (PEMC), September, pp. 1310-1318, 1994.
- [12]. Santosh A and Shivashankar Tallada , Simulation Of High-Efficiency AC/DC Converter For Power Factor Correction - International Journal of Engineering Research and Applications(IJERA)ISSN:2248-9622, Vol. 2, Issue4, pp.2043-2050, 2012.